SLM High Speed Access and Test

Leverage existing functional interfaces to access DFT or SLM network over entire silicon lifecycle

Highlights

- Reuse HSIO interfaces such as PCIe or USB for test and other data avoiding the need for very large numbers of test pins
- Speed up test by exceeding GPIO test pin data rates
- Easily repeat manufacturing tests in-system and in-field
- Enhance testing in-system and in-field with updated tests
- High speed access to PVT monitors, debug and other sensor data
- Bandwidth scales with each new generation of HSIO (PCIe, USB)

Target Applications

- Large SoCs with high test volume and pin limitations
- Applications where in-field reliability is key
- High performance compute, AI and server
- Desktops, notebooks and workstations
- Industrial, automotive and IoT
- Smartphones and 5G Infrastructure

Overview

Synopsys SLM High-Speed Access and Test (HSAT) IP combined with Synopsys TestMAX® ALE software uses standard high speed IO interfaces such as PCIe and USB, to get test, debug and monitoring data in and out of an SoC at Gigabit data rates and avoids the need for large numbers of test and interface pins. Test time can be reduced because the link between the test time and GPIO data rate is eliminated. Further, this solution provides a key component for Synopsys Silicon Lifecycle Management solution allowing manufacturing tests to be repeated in-system and in-field as well as providing high speed access to PVT and functional monitor data.

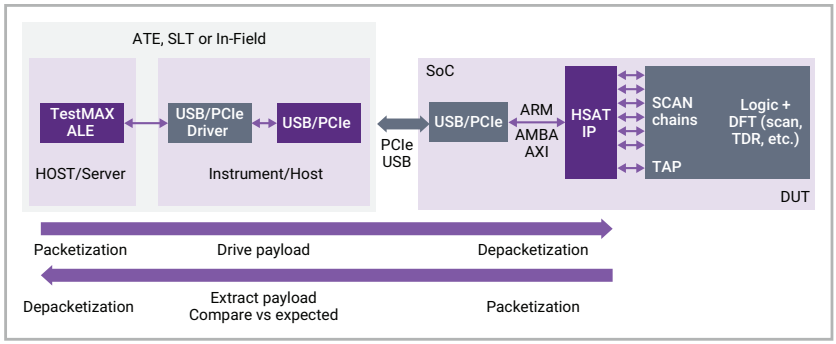


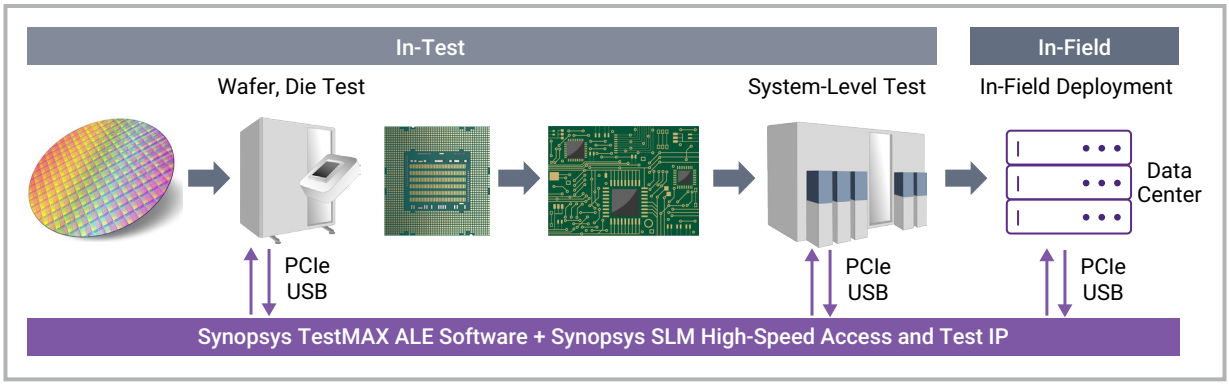
Figure 1: Synopsys SLM High-Speed Access and Test IP and Synopsys TestMAX ALE Solution

Key Features

- PCIe, USB high speed IO for ATE, in-system and in-field
- Can use other available interfaces (e.g. SPI) for in-system/in-field
- Configurable Arm® AMBA® AXI slave interface to HSIO
- Configurable number of scan chains (512 max) and TAP port supported
- Full RTL configuration and integration flow
- Arm AMBA AXI testbench generation
- Optional EBC interface for USB
- Bypass mode allows scan chains to connect to HS Access or GPIO pins
- Multiple levels of loop back for link validation

Key Benefits

- Reduce test time by eliminating the constraint of GPIO test pin data rate
- Re-use functional HSIO ports (PCIe and USB) for test and other data
- Avoid the need for large numbers of GPIO test pins
- Easily repeat manufacturing structural tests in-system and in-field
- High speed access to PVT and functional monitors and other sensor data
- Bandwidth scales with each new generation of PCIe/USB



Manufacturing Test—Reduce Test Time and Number of Test Pins

Synopsys SLM HSAT IP combined with the Synopsys TestMAX ALE software tool, enables the functional HSIO ports to be reused to get test and other data in and out of an SoC at Gigabit data rates. This eliminates the constraint on test time typically imposed by slow GPIO test pin data rates enabling test time to be reduced. It also avoids the need for very large numbers of GPIO test pins.

In-System and In-Field—Repeat Manufacturing Structural Tests

Once the Synopsys SLM HSAT IP is instantiated on an SoC and test data packets prepared by Synopsys TestMAX ALE the manufacturing tests can be repeated in-system and in-field simply by switching the SoC to a test mode and transmitting the same packets over the HSIO (PCIe or USB). In-field the SoC will not know it is no longer connected to the ATE tester and will carry out the same manufacturing tests. Tests can be updated in-field by simply updating the data packets to be sent over the HSIO. PVT and functional monitor data can also be accessed at high speed in-field using this solution.

Implementation—Easily Configure, Instantiate and Verify the IP in your SoC

Synopsys SLM HSAT IP is part of the Synopsys Silicon Lifecycle Management Family and is easily configured and generated and optionally instantiated using Synopsys TestMAX Manager or customer's own integration method or manually. Configuration includes setting the number of scan chains, configuring the Arm® AMBA® AXI interface and a few other parameters. As part of the flow a test bench is automatically produced for the Arm® AMBA® AXI interface.

Synopsys TestMAX ALE—Prepares and Processes Data Packets Communicated over the HSIO

Synopsys TestMAX ALE is a software tool and takes standard scan test data in the IEEE 1450 (STIL) format and prepares data payloads (HS Access packets) for communication over the HSIO (PCIe or USB). On the SoC these data packets are then depacketized and fed to the hundreds of scan chains and TAP port. Scan chain results are similarly fed back from the SoC to the ATE tester with the packetization this time performed by the HSAT IP and depacketization on the tester side performed by Synopsys TestMAX ALE. Synopsys TestMAX ALE can be run offline and test data packets prepared in advance which are then used either in ATE test or later in field. This example is for test, but Synopsys TestMAX ALE + HSAT IP can be also used for other data such as accessing PVT and functional monitor data from the SoC.

About Synopsys IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad Synopsys IP portfolio includes logic libraries, embedded memories, PVT sensors, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors, and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits, and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market.

For more information on Synopsys IP, visit synopsys.com/ip.

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